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(71) Applicant: 000005821
Matsushita Electric Industrial Co. Ltd.
1006, Oaza Kadoma, Kadoma-shi, Osaka

(72) Inventor: Hiroshi Haji
Matsushita Electric Industrial Co. Ltd.
1006, Oaza Kadoma, Kadoma-shi, Osaka

(72) Inventor: Shoji Sakemi
Matsushita Electric Industrial Co. Ltd.
1006, Oaza Kadoma, Kadoma-shi, Osaka

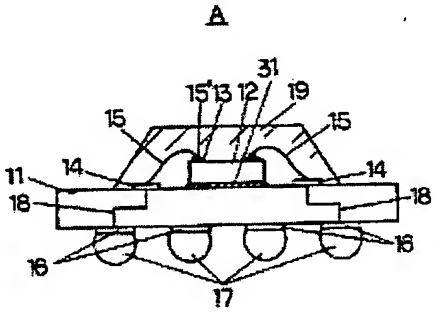
(74) Agent: Tomoyuki Takimoto, Patent attorney (and 1 other)

(54) Title of the Invention: Method of Manufacturing an Electronic Component

(57) Abstract

Problem to be solved: To provide an electronic component assembly method capable of bonding a gold wire and forming a solder bump favorably on a copper pad on a substrate.

Solution: On copper pads 21 and 24 of a substrate 11 are formed nickel films 22 and 25, and gold films 23 and 26 are formed additionally thereupon. In order to inhibit the formation of a gold-tin compound which degrades the reliability of solder, the gold films 23 and 26 are formed on the nickel films 22 and 25 using an ultra-thin substitutional plating method. As a result, the solder bumps 17 can be formed favorably. Also, the nickel oxide film 32 formed on the surface of the gold film 23 is removed by plasma etching prior to performing wire bonding. As a result, the bonding of a wire 15 can also be performed favorably.



11 Substrate
12 Chip
14, 16 Pad
15 Wire
17 Solder bump

Claims

Claim 1

A method of manufacturing an electronic component, comprising the steps of:

forming a copper pad for bonding a gold wire to the surface of a substrate and forming a copper pad for forming a solder bump;

forming a metal barrier layer comprised of at least nickel film on each of these copper pads;

forming a gold film on each metal barrier layer;

mounting a chip on the substrate with thermosetting adhesive and applying heat to affix [the chip on the substrate];

plasma etching to remove nickel oxide film formed on the surface of the gold film due to the application of heat;

bonding a wire to the surface of the plasma-etched gold film, and then electrically connecting the chip and the copper pad covered by the gold film;

forming, on the surface of the substrate, molded resin that seals the chip and wire; and

forming a solder bump on said copper pad for forming a solder bump.

Detailed Explanation of the Invention

[0001]

Relevant Technical Field of the Invention

The present invention relates to a method of manufacturing an electronic component.

[0002]

Prior Art

A structure in which a wire is bonded onto a pad on the surface of a substrate in order to connect the substrate and a chip, and a bump is formed as a protruding electrode on top of another pad, is a known electronic component assembly structure. The ball grid array (BGA) package is known as such an electronic component. Gold wire is commonly used for the wire, and solder is commonly used for the bump.

[0003]

FIG. 9 is a cross-sectional drawing of a conventional substrate. In the drawing, reference numeral 1 indicates a substrate of glass epoxy or the like, having circuit pattern copper pads 2 and 3 formed on its upper and lower surfaces. Nickel films 4 and 5 are formed on the copper pads 2 and 3, and gold films 6 and 7 are formed on the nickel films 4 and 5. An internal wire 8 connects the upper copper pad 2 and lower copper pad 3. The tip of a gold wire 9 for connecting a chip (not shown) mounted on the substrate 1 is bonded to the top of the gold film 6 of one copper pad 2, and a solder bump 10 is formed on top of the gold film 7 of the other copper pad 3, thereby assembling an electronic component.

[0004]

The nickel films 4 and 5 and gold films 6 and 7 are generally formed by plating. The gold films 6 and 7 are formed for the purpose of enhancing the bonding performance of the gold wire 9. Conventionally, the gold films 6 and 7 had a thickness of about 0.3 to 1 micron, which is considerably thick. The nickel films 4 and 5 are formed as a metal barrier to prevent the copper material of the copper pads 2 and 3 from diffusing into the gold films 6 and 7, and forming an oxide film when exposed to air. If an oxide film forms on the surface of the gold film 6, the bonding of gold wire 9 will be unsatisfactory.

[0005]

Problem to be Solved by the Invention

In the above-described conventional method, during the process for affixing the chip, heating of the metal barrier nickel films 4 and 5 causes the nickel constituent thereof to diffuse

into the gold films 6 and 7. This diffused nickel is exposed to air at the surface of gold films 6 and 7 and forms oxide film. Because this oxide film impairs the bonding of the gold wire 9, it was previously necessary to make the thickness of gold films 6 and 7 greater than a certain thickness in order to prevent the formation of this oxide film as much as possible. However, increasing the thickness of the gold films 6 and 7 decreases the bonding strength of the solder bump 10. This is because, when forming the solder bump 10, the gold in the gold film 7 melts into the solder bump 10 and combines with tin in the solder to form a brittle compound. Thus, it is preferable that one gold film 6 is thick for the purpose of bonding the gold wire 9 and that the other gold film 7 is thin for the purpose of forming the solder bump 10, and this contradictory relationship was a problem. FIG. 9 shows the gold film 7 on the copper pad 3, but in actuality, the majority of this gold film 7 will melt into the solder bump 10 and will not remain on the surface of the nickel film.

[0006]

The abovementioned problem does not occur, however, in the case of a substrate type provided with pads formed with solder bumps only, without the bonding of a gold wire. This is because, when forming a solder bump only, a two-layer structure consisting of a gold film formed directly on a copper pad may be used, without the formation of a nickel film. Namely, in this case, the copper material of the copper pad diffuses into the gold film and, when exposed to external air, generates an oxide film that impairs the bonding performance of the solder bump as described above. However, flux is used when forming the solder bump, and this flux reduces and removes the oxide film. Thus, the abovementioned problem is specific to cases in which an electronic component is assembled by bonding a gold wire to the top of a copper pad on the substrate and by forming a solder bump on another copper pad.

[0007]

Accordingly, it is an object of the present invention to provide an electronic component assembly method capable of bonding a gold wire and of forming a solder bump favorably on copper pads on a substrate.

[0008]

Means For Solving the Problem

A method of assembling an electronic component according to the present invention comprises the steps of: forming a copper pad for bonding a gold wire to the surface of a substrate and forming a copper pad for forming a solder bump; forming a metal barrier layer comprised of at least nickel film on each of these copper pads; forming a gold film on each metal barrier layer with a substitutional plating method; mounting a chip on the substrate with thermosetting adhesive and applying heat to affix [the chip on the substrate]; plasma etching to remove nickel oxide film formed on the surface of the gold film due to the application of heat; bonding a wire to the surface of the plasma-etched gold film, and then electrically connecting the chip and the copper pad covered by the gold film; forming, on the surface of the substrate, molded resin that seals the chip and wire; and forming a solder bump on the copper pad for forming a solder bump.

[0009]

Embodiment of the Present Invention

According to the present invention having the above-described configuration, prior to bonding, the nickel compound that impairs bonding of the gold wire is removed from the surface of the gold film by plasma cleaning. Consequently, the gold film can be made much thinner than in the past, and bonding of the gold wire and formation of the solder bump can be implemented favorably.

[0010]

An embodiment of the present invention is described below with reference to drawings. FIG. 1 is a view of the assembly structure of an electronic component in an embodiment of the

present invention; FIGS. 2 and 3 are cross-sectional views of the same substrate; FIG. 4 is a partial cross-sectional view of the same substrate; FIG. 5 is a cross-sectional view of the same[1] plasma etching apparatus; and FIGS. 6, 7 and 8 are cross-sectional views of the same substrate.

[0011]

First, the structure of an electronic component A is described. In FIG. 1, reference numeral 11 indicates a substrate onto the top of which a chip 12 is bonded with a thermosetting adhesive 31. A pad 13 on the surface of the chip 12 and a pad 14 on the top surface of the substrate are electrically connected by a gold wire 15. Reference number 15' indicates a gold ball formed at a tip of the gold wire, and this gold ball 15' is bonded to the pad 13.

[0012]

On the bottom surface of the substrate 11, a pad 16 is formed. A solder bump 17 is formed on the pad 16. An internal wire 18 connects the pads 14 and 16. The top surface of the substrate 11 is provided with molded resin 19 in order to seal the chip 12 and the gold wire 15.

[0013]

Next, a method of manufacturing the electronic component shown in FIG. 1 is described with reference to FIGS. 2 through 8. FIGS. 2 through 8 are shown in the sequence of the manufacturing process. FIG. 2 shows a cross-sectional view of the substrate 11. The upper pad 14 is formed by coating a copper pad 21 with a nickel film 22 as a metal barrier layer, and then by coating the nickel film 22 with an extremely thin gold film 23. Additionally, the lower pad 16 is similarly formed by coating a copper pad 24 with a nickel film 25, and then coating the nickel film 25 with an extremely thin gold film 26. Gold films 23 and 26 are formed by a substitutional plating method and have thicknesses ranging from approximately 0.03 to 0.05 microns, which is much thinner than previous thicknesses (of 0.3 to 1 micron as mentioned above). The upper gold film 23 is provided in order to ensure the bonding strength of the gold wire.

[0014]

In FIG. 3, reference numeral 12 indicates a chip. The chip 12 is mounted on the top surface of the substrate 11, and is adhered by a thermosetting adhesive 31 applied in advance on the top surface of the substrate 11. The substrate 11 is then heated. Curing the thermosetting adhesive 31 causes the chip 12 to become affixed to the substrate 11.

[0015]

FIG. 4 is a cross-sectional view of a region in the vicinity of pads 14 and 16 on the substrate 11 after this heat treatment has been performed. Reference numerals 32 and 33 indicate nickel oxide films formed on the surface of the gold films 23 and 26 of the pads 14 and 16. These nickel oxide films 32 and 33 are formed when nickel, which has gradually diffused into gold films 23 and 26, comes into contact with air at the surface of the gold films 23 and 26 during the heat treatment. As described above, the nickel oxide film 32 formed on the top pad 14 side impairs the bonding performance of the gold wire. On the other hand, the nickel oxide film 33 formed on the bottom pad 16 side is reduced and removed by flux applied in a later process, and therefore has no adverse effect on the adhesion of the solder bump 17.

[0016]

Next, plasma etching is performed to remove the nickel oxide film 32 at the pad 14 side. The structure of a plasma etching apparatus 40 used in this plasma etching is described below with reference to FIG. 5. In FIG. 5, reference numeral 41 indicates an upper casing. The upper casing 41, together with a lower casing 42, form a vacuum container 43 that may be opened and closed. An electrode 44 is disposed at the bottom of the lower casing 42. A high frequency power supply apparatus 45 is connected to the electrode 44. Pipes 46, 47 and 48 are provided at the bottom surface of the lower casing 42. A vacuum source 49 is connected to the pipe 46.

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[1] Translator's note: The use of "same" here is unclear. There is no prior reference to a plasma etching apparatus.

Additionally, a gas supply unit 50 that supplies plasma-etching gas such as argon gas is connected to the pipe 47. Furthermore, a vacuum break valve 51 is attached to the pipe 48.

[0017]

An earth electrode 52 is mounted at the top portion of the upper casing 41. The earth electrode 52 is connected to a grounding unit 53 and is installed at a location opposite the electrode 44. The substrate 11 is mounted on the electrode 44.

[0018]

This plasma etching apparatus 40 has a configuration as described above and its operation is described below. With the substrate 11 mounted on the electrode 44 as shown in FIG. 5, the upper casing 41 is closed. Then, the vacuum source 49 initiates a vacuum suction and the inside of the vacuum container 43 reaches a specified degree of vacuum. Next, the gas supply unit 51 supplies argon gas into the vacuum container 43 and the high-frequency power supply apparatus 45 applies a high frequency voltage to the electrode 44. The argon gas inside the vacuum container 43 forms an argon ion plasma that collides with the top surface of the substrate 11 mounted on the electrode 44 as indicated by the broken-line arrow in FIG. 5 to accomplish the etching. In this manner, the nickel oxide film 32 is removed from the surface of the pad 14. In this case, argon ions also collide with the surface of the substrate 11 in addition to the surface of the pad 14. As a result, the surface of the substrate 11 is roughened, thereby increasing the surface roughness. The effect of this surface roughness is described later.

[0019]

After the nickel oxide film 32 has been removed from the pad 14 side in this manner, the gold wire 15 is then bonded onto the gold film 23 of the upper pad 14 as shown in FIG. 6. Next, the molded resin 19 as shown in FIG. 7 seals the chip 12 and the gold wire 15. In this case, as was described above, the degree of roughness on the surface of the substrate 11 has been increased due to the plasma etching. This roughened surface is used an anchor, and it increases the adhesion between the substrate 11 and the molded resin 19.

[0020]

Next, as shown in FIG. 8, the substrate 11 is turned upside down, and a solder ball 17 is mounted on the gold film 26 of the pad 16 side. At this time, flux 20 is applied between the solder ball 17 and the gold film 26. Then, the substrate 11 is sent to a reflow process, the solder ball 17 is soldered to the pad 16 surface, and the solder ball 17 becomes a solder bump 17, thereby completing the electronic component A shown in FIG. 1. At this time, the nickel oxide film 33 formed on the gold film 26 (see FIG. 4) is reduced by the flux 20 and is melted into the solder bump 17 so that it has no effect on the bonding performance of the solder bump 17. The gold film 26 also melts into the solder bump 17, but since the film thickness is extremely thin as described above, only a very small amount is melted into the solder bump 17. Thus, a highly reliable solder bump 17 is formed without impairing the bonding performance of the solder bump 17. Additionally, since the gold films 23 and 26 can be made extremely thin, the usage of gold, which is an expensive material, can be reduced dramatically, thereby enabling a significant decrease in the manufacturing cost of the electronic component.

[0021]

Effect of the Invention

In the present invention, because the nickel compound that impairs bonding of the gold wire is removed from the surface of the gold film prior to bonding, a dramatic cost reduction can be achieved by making the gold film much thinner than in the past, thereby enabling a significant reduction in the manufacturing cost of the electronic component. Moreover, bonding of the gold wire and formation of the solder bump can be implemented favorably, thereby enabling a highly reliable electronic component to be obtained.

Brief Explanation of the Drawings

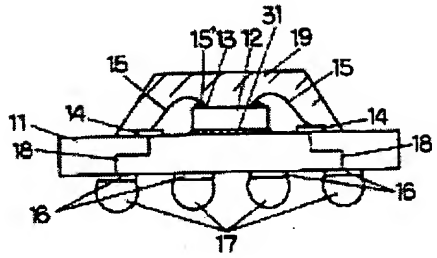
FIG. 1 is a view of the assembly structure an electronic component in an embodiment of the present invention.
FIG. 2 is a cross-sectional view of a substrate in an embodiment of the present invention.
FIG. 3 is a cross-sectional view of a substrate in an embodiment of the present invention.
FIG. 4 is a partial cross-sectional view of a substrate in an embodiment of the present invention.
FIG. 5 is a cross-sectional view of a plasma etching apparatus in an embodiment of the present invention.
FIG. 6 is a cross-sectional view of a substrate in embodiment of the present invention.
FIG. 7 is a cross-sectional view of a substrate in embodiment of the present invention.
FIG. 8 is a cross-sectional view of a substrate in embodiment of the present invention.
FIG. 9 is a cross-sectional view of a conventional substrate.

Explanation of the Reference Numerals

11 Substrate
12 Chip
14, 16 Pad
15 Wire
17 Solder bump
23, 26 Gold film
32, 33 Oxide film

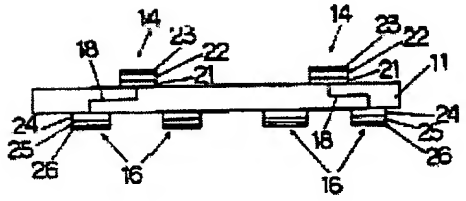
FIG. 1

A



11 Substrate
12 Chip
14, 16 Pad
15 Wire
17 Solder bump

FIG. 2



23, 26 Gold film

FIG. 3

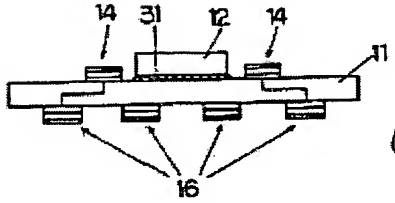
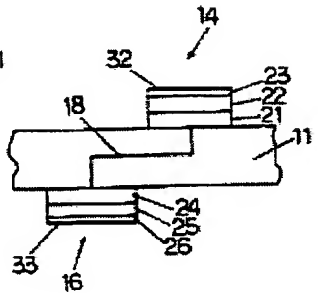


FIG. 4



32, 23 Oxide film

FIG. 5

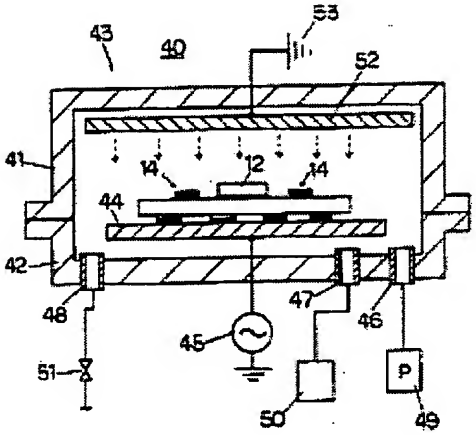


FIG. 6

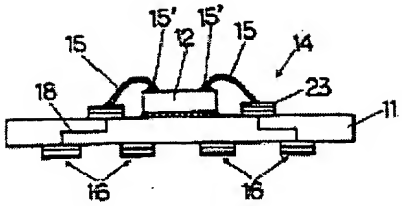


FIG. 9

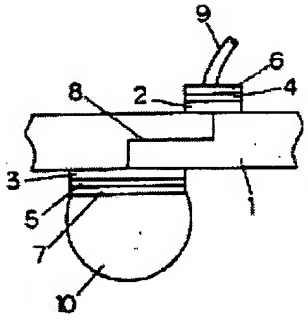


FIG. 7

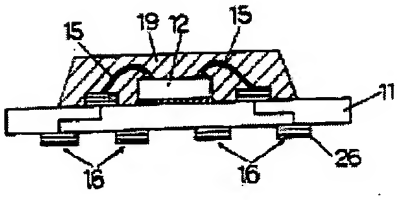


FIG. 8